AMENDMENTS TO THE CLAIMS

Please amend the claims of the present application as set forth below.

1. (Currently Amended) A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, said first and second transistors being respectively a PFET and an NFET, each of said transistors including a gate electrode and a source drain path arranged to be switched on and off in response to a voltage applied to the gate electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, and pulse shaping circuitry for(a) causing the first and second source drain paths to be respectively (i) on and off while the voltage source has the first level and (ii) of and on while the voltage source has the second level, and (b) preventing both source drain paths from being on simultaneously, the pulse shaping circuitry including a resistive element and a capacitor, the resistive element being connected for supplying current to the capacitor and the gate electrode ~~of the first transistor, the capacitor being connected across the gate electrode of one of said transistors~~ of one of said transistors, the capacitor being connected across the gate electrode of said one of said transistors and a first of the power supply terminals, the first power supply terminal being connected for supplying current to the source drain path of the other of said transistors while the source drain path of the other of said transistors in on, the capacitor comprising a field

effect device having a conductivity type opposite to the conductivity type of said one of the said transistors[[.]];

wherein the pulse shaping circuitry includes a switching circuit having (a) an input terminal for enabling the switching circuit to be responsive to the voltage at the first terminal and(b) an output terminal, the output terminal of the switching circuit being connected so current can flow via a DC path between (a) the first power supply terminal and (b) the capacitor and the gate electrode of said on transistor, the DC path including the resistive element;

wherein the switching circuit includes an inverter having field effect transistors;

wherein all the field effect transistors of the inverter are included on an integrated circuit chip including a resistor comprising the resistive element connected with said one field effect transistor and the inverter;

wherein the resistor is included in the inverter;

wherein the field effect transistors of the inverter include another PFET and another NFET, the another PFET and another NFET of the inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the another PFET and another NFET of the inverter are arranged to be driven in parallel by the voltage at the first terminal, the output terminal of the inverter being between the source drain paths of the another PFET and the another NFET; and

wherein the resistor is connected between the source drain path of the NFET of the inverter and output terminal of the inverter, the source drain path of

the another PFET of the inverter being connected directly between the output terminal of the inverter and one of the power supply terminals that the voltage at the one power supply terminal is always applied directly to the output terminal of the inverter via the source drain path of the another PFET of the inverter, while the source drain path of the another PFET of the inverter is switched on.

2. (Canceled)

3. (Previously presented) The circuit of claim 1 wherein said resistive element, PFET, NFET and said capacitor are included on an integrated circuit chip, and said resistive element comprises a resistor.

4-13. (Canceled)

14. (Previously Presented) A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each of the transistors including a control electrode and a path switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite first and second power supply terminals, an output terminal between the paths, pulse shaping circuitry connected between the input terminal and the control electrodes for (a) causing the paths of the first and second transistors to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing the paths of the first and second transistors from being on simultaneously, the pulse shaping circuitry including: (a) first and second switching circuits arranged to be connected to be simultaneously responsive to the voltage at the voltage at the first terminal, the first and second switching circuits respectively including output terminals that are DC connected to the control electrodes of the first and second transistors; and (b) first and second capacitors that are respectively DC connected between(i) the first control electrode and the first power supply terminal and (ii) the second control electrode and the second power supply terminal, the first switching circuit including a first resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and the first capacitor while the voltage at the first terminal has the first level, the first

switching circuit being arranged for supplying a voltage substantially equal to the voltage at the second power supply terminal to (i) the control electrode of the first transistor and (ii) the first capacitor while the voltage at the first terminal has the second level; the second switching circuit including a second resistive element for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the voltage at the first terminal has the second level, the second switching circuit being arranged for supplying a voltage substantially equal to the voltage at the first power supply terminal to (i) the control electrode of the second transistor and (ii) the second capacitor while the voltage at the first terminal has the first level, the first switching circuit further comprising: a first inverter including third and fourth transistors respectively connected to be switched on and off in response to the voltage at the first terminal respectively have first and second values, the first inverter including the first resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and first capacitor while the third transistor is switched on; the second switching circuit further comprising a second inverter including fifth and sixth transistors respectively switched on and off in response to the voltage at the first terminal respectively having first and second values, the second inverter including the second resistive element for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the sixth transistor is switched on, wherein the transistors of each of the inverter including a PFET and NFET, the PFET and NFET of each

inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are arranged to be driven in parallel by the voltage at the first terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof, the first resistive element being connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, the second resistive element being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

15. (Cancelled)

16. (Previously presented) The circuit of claim 14 wherein the fourth and fifth transistors while switched on are connected to supply voltages substantially at the second and first power supply terminals to the control electrodes of the first and second transistors and the first and second capacitors, respectively.

17. (Original) The circuit of claim16 wherein all the transistors and capacitors are field effect devices.

18. (Previously presented) The circuit of claim 17 wherein all the transistors and capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

19.-21. (Canceled)

22. (Previously presented) The circuit of claim14,wherein the first resistive element is connected between the source drain paths of the PFET and NFET of the first inverter, and the connection of the first resistive element to the PFET and NFET of the first inverter is such that substantial current flows through the first resistive element while the NFET of the first inverter is switched on and insubstantial current flows through the first resistive element while the PFET and PFET of the first inverter are respectively switched off and on, and the second resistive element is connected between the source drain paths of the PFET and NFET of the second inverter and the connection of the second resistive element to the NFET and PFET of the second inverter is such that substantial current flows through the second resistive element while the PFET of the second inverter is switched on and insubstantial current flows through the second resistive element while the PFET ad NFET of the second inverter are respectively switched off and on.

23. (Canceled)

24. (Canceled)

25. (Currently Amended) The circuit of claim [[11]] 1, wherein the resistor is connected between the source drain path of the another PFET of the inverter and the output terminal of the inverter, the source drain path of the another NFET of the inverter being connected directly between the output terminal of the inverter and the one of the power supply terminals that the voltage at the one power supply terminal is always applied directly to the output terminal of the inverter via the source drain path of the another NFET of the inverter, while the source drain path of the another NFET of the inverter is switched on.

26. (Previously Presented) The circuit of claim 25, wherein the resistor is connected between the source drain paths of the another NFET and another PFET of the inverter, and the connection of the resistor to the another NFET and another PFET of the inverter is such that substantial current flows through the resistor while the another PFET is switched on an insubstantial current flows through the resistor while the another PFET is switched on and the another NFET is switched off.

27. (Previously Presented) The circuit of claim 1, wherein the voltage source has transitions in both directions between the first and second source levels, the pulse circuitry being arranged for preventing both source drain paths from being on simultaneously in response to the transitions in both directions.

28. (Currently Amended) A circuit comprising a first signal terminal for connection to a voltage source having first and second levels and a transition between the first and second levels, a PFET transistor and an NFET transistor, said PFET and NFET transistors each including a gate electrode and a source drain path arranged to be switched on and off in response to a voltage applied to the gate electrode thereof being on opposite sides of a threshold between the first and second levels, the source drain paths being connected in series between first and second opposite DC power supply terminals, the first power supply terminal being adapted to be connected to a first DC voltage for supplying DC power supply current directly to the source drain path of the PFET transistor without directly supplying DC power supply current to the NFET transistor, the second power supply terminal being adapted to the connected to a second DC voltage for supplying DC power supply current directly to the source drain path of the NFET transistor without directly supplying DC power supply current to the PFET transistor, an output terminal connected between the source drain paths of the PFET and NFET transistors to be respectively (a) on an off in response to the voltage source having the first level and (b) off an d on in response to the voltage source having the second level, the pulse shaping circuitry including a first resistive element and a first capacitor, the first resistive element being connected to be responsive to the voltage at the first signal terminal for directly supplying current to the first capacitor and the gate electrode of a first of the transistors without directly supplying current to the gates electrode of the second of the transistors, the capacitor being a FET

device having a conductivity type opposite from that of the first of the transistors and including first and second electrodes connected between the gate electrode of the first of the transistors and the power supply terminal for supplying current directly to the source drain path of the second of the transistors[[.]];

wherein the voltage source has transitions in both directions between the first and second levels, the first DC voltage having an amplitude greater than the amplitude of the second DC voltage, the first and second of the transistors being respectively the PFET and NFET transistors so that the first capacitor is an NFET device having a first electrode connected to the second power supply terminal, the pulse shaping circuitry being arranged for preventing both source drain paths from being on simultaneously in response to the transitions in both directions, the pulse shaping circuitry further including a second resistive element connected to be responsive to the voltage at the first signal terminal and a second capacitor, the first resistive element and the first capacitor being connected for directly supplying current to the gate electrode of the PFET transistor without directly supplying current to the second capacitor and the gate electrode of the NFET transistor, the second resistive element being connected for supplying current to the second capacitor and the gate electrode of the NFET transistor without directly supplying current to the first capacitor and the gate electrode of the PFET transistor, the second capacitor being a PFET device having a first electrode connected between the gate electrode of the NFET transistor and a second electrode connected to the first power supply terminal.

29. (Canceled)

30. (Previously Presented) A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including a first PFET and a fist NFET, each of the transistors including a gate electrode and a source drain path arranged to be switched on and off in response to a voltage applied to the gate electrode being on opposite sides of a threshold, the PFET and NFET paths being connected in series across opposite first and second DC power supply terminals, the first power supply terminal being adapted to be connected to a positive DC power supply voltage, first and second inverters connected to be driven in parallel by the voltage source at the first terminal, the first inverter including (a) a second PFET and a second NFET having series connected source drain paths connected across the first and second DC power supply terminals, (b) a first resistive element coupled in series with the source drain path of the second NFET, (c) an output terminal connected between the drain electrode of the second PFET and the first resistive element, the second inverter including (a) a third PFET and a third NFET having series connected source drain paths connected across the first and second DC power supply terminals, (b) a second resistive element connected in series with the source drain path of the third PFET, (c) an output terminal connected between the drain electrode of the third NFET and the second resistive element; a first DC path connected between the output

terminal of the first inverter and the gate of the first PFET; a second DC path between the output terminal of the second inverter and the gate of the first NFET; a first capacitor connected in a first shunt path between the first DC path and the second power supply terminal; and a second capacitor connected in a second shunt path between the second DC path and the first power supply terminal.

31. (Previously Presented) The circuit of claim 30 wherein the first capacitor includes a field effect device having a conductivity opposite to that of the first PFET and the second capacitor includes a field effect NFET device.

32. (Previously Presented) The circuit of claim 31, wherein the first and second resistive elements comprise firs and second resistors, respectively.